

### Systems Development SDD-602A Video Graphic Processor

#### Features

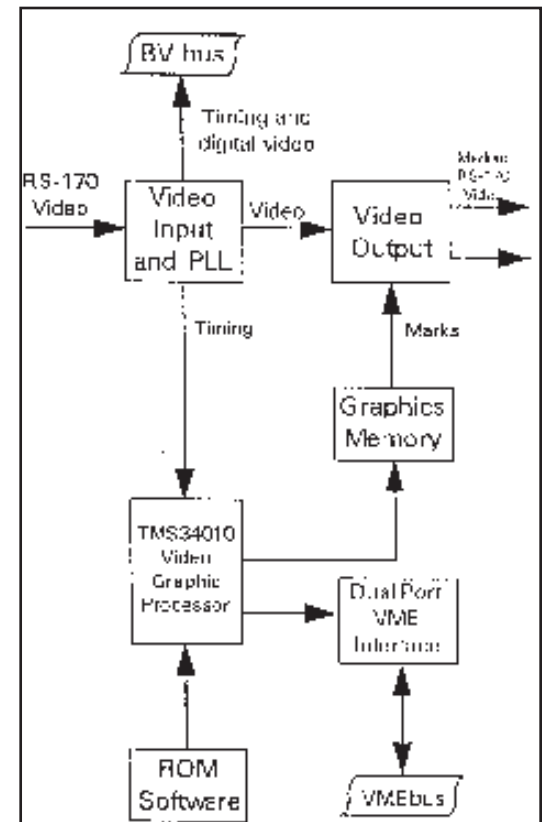
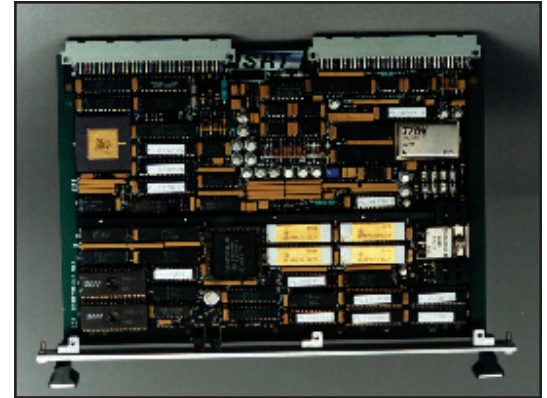
- Ideal for Real-Time Field Rate Applications
- Significantly reduces software development time
- Complete with standard commands, fonts, and drives
- User fonts configurable for downloading
- TMS 34010 Video Graphic Processor
- Two, 512 x 512 x 1-bit graphics overlay planes
- Marks generation software included on board
- Optional video sync and blanking regeneration
- Full 8-bit, 10 MHz video digitization
- BVbus timing and data master

#### Description and Operation

The Systems Development Department (SDD) has developed the SDD-602A Video Graphic Processor (VGP) as a single-board, high-performance, graphic processor and video digitizer. The VGP has two independent graphic planes for real-time marks insertion onto the incoming RS-170 video. The graphics planes can be OR'ed together to simplify the operations to display rapidly changing data with static background data.

The VGP is controlled by a high-speed video graphic processor, which generates the text and graphics for overlay, and controls the low level operations of the board. The VGP interfaces to a host processor through a high-level, DPRAM VME interface. Dedicated locations in this DPRAM contain board identification, operating status, and a command string for the graphics overlay. The command string consists of a sequence of high level commands to the VGP, such as "Draw Line", "Draw Box", "Draw Crosshair #3"(one of 27 types), Write Text, and various mode selection commands. Execution of the command string is started by writing to a dedicated location.

The video input section of the VGP accepts standard RS170 video. A phase-locked-loop (PLL) automatically synchronizes to the incoming video. The PLL generates all video timing for use within the VGP, and for transmission over the BVbus interface. In the absence of incoming video, the PLL will free run so that marks can be produced without an external video source. The VGP has the option of regenerating video timing information in the output video channels. The incoming video is digitized to 8-bit gray scale resolution at 10 MHz by a flash A/D converter. This video data is output over the BVbus interface for use by other BVbus compatible processing boards.



SDD-602A Block Diagram

## Specifications

### FUNCTIONAL

#### Major Components

- TMS34010 Video Graphic Processor
- 40 MHz Video phase locked loop
- Dual port RAM, VME bus interface
- Graphics Memory
- Analog RS-170 video input and outputs
- BVbus digital video timing and data outputs
- Graphics generating software

#### VME Interface

- 1 K x 16 bit dual port RAM with dedicated status information and command string areas

#### Graphics Overlay

- Marks memory for each frame: 512 pixels per line, 512 lines per field, 1 bit per pixel
- Bright marks or dark marks, software selectable
- 2 planes in which marks can be written independently, and which can be OR'ed together for display
- Display of marks can be disabled for each plane independently
- 2 frame buffers for each plane, which allow data to be written asynchronously to vertical sync, so that the visible marks will change only on field boundaries.

#### Digitization of Video

- 8-bit gray scale resolution per pixel
- 616 pixels per horizontal line time, giving 512 pixels of active video per line at approximately 103 ns per pixel

#### Timing

- Automatic synchronization with incoming video by the use of a phase locked loop circuit
- Generation of video timing signals for BVbus
- Operational regeneration of video sync and blanking in the output video
- Free-run in the absence of an input video signal

## ELECTRICAL

### Analog Video

- 1 input, 2 buffered outputs (one for each plane ofmarks)
- RS-170 standard video, monochrome, 1.0 or 1.4 Volt, black negative, negative going sync
- Jumper selectable interlacing and field rates: 60 Hz field, 525 lines/frame, interlaced or non-interlaced 50 Hz field, 625 lines/frame, interlaced or non-interlaced
- Jumper selectable input termination: 75 Ohms or high impedance
- 75 Ohms output impedance for both output channels

### BVbus

- BVbus timing master
- BVbus data source; generates 8-bit digital video data at 10MHz

### VME Bus

- Complies with VME bus specification: ANSI/IEEE STD 1014-1987
- A16:D16 DTB Slave
- Interrupter: Jumper selectable to level 1 through 7, status ID is programmable
- Form Factor: single width, double height, 6 U
- Word addressable
- Jumper selectable bus address: Short I/O space, on addresses 0x0000 through 0xF800, on multiples of 0x0800

### Power

- +5V @ 2.75A
- +12V @ 0.25A
- 12V @ 0.50A

### OPTIONS

- Full Mil-Spec Hardware
- Ruggedized Hardware
- Custom Marks Commands
- Custom Power-up Screen Marks
- Other custom software changes

### For more information, please contact:

Gary West  
Director  
205-581-2267  
west@sri.org

John Collier  
Program Manager  
205.581.2508  
collier@sri.org

## SOUTHERN RESEARCH

Legendary Discoveries. Leading Innovation.

Birmingham Alabama | 800.967.6774 | www.SouthernResearch.org